

IN THE CLAIMS

Please cancel claims 10-19 and add new claims 20-43 as set forth below.

1. - 19. (Canceled)

20. (New) A computer system which enlarges an image represented by image signals to be displayed, comprising:

a computer main unit which outputs said image signals and first horizontal synchronizing signals;

a memory which is arranged to store said image signals;

a display panel which displays said image represented by said image signals;

a processing circuit which enlarges said image represented by said image signals by a non-integer number of times in accordance with a resolution of said display panel divided by a resolution of said image represented by said image signals outputted from said computer main unit; and

a control circuit which inputs said image signals into said memory in accordance with said first horizontal synchronizing signals which have been inputted together with said image signals, and outputs said image signals from said

memory in accordance with second horizontal synchronizing signals synchronized with said first horizontal synchronizing signals,

wherein said control circuit synchronizes said second horizontal synchronizing signals with said first horizontal synchronizing signals, every time one of said first horizontal synchronizing signals is generated M times and one of said second horizontal synchronizing signals is generated N times,

N is not equal to M,

N divided by M is a non-integer number,

N divided by M corresponds to the resolution of said display panel divided by the resolution of said image represented by said image signals outputted from said computer main unit, and

a generation cycle of one of said second horizontal synchronizing signals is almost constant.

21. (New) A computer system according to claim 20, wherein said memory is arranged to store said image signals for one frame.

22. (New) A computer system according to claim 20, wherein said memory is arranged to store said image signals for two lines.

23. (New) A computer system according to claim 20, wherein said processing circuit generates data which should be inserted into said image signals with a tone integral method.

24. (New) A computer system according to claim 20, further comprising:

a timing-generating circuit which generates display timing signals used on said display panel, based on said first horizontal synchronizing signals and vertical synchronizing signals which have been inputted together with said image signals,

wherein said timing-generating circuit inputs said image signals whose image has been enlarged, and outputs said image signals on said display panel together with said display timing signals.

25. (New) A computer system according to claim 24, wherein said timing-generating circuit comprises:

a synchronizing circuit which synchronizes said first horizontal synchronizing signals with a standard clock, and

a generating circuit which generates said second horizontal synchronizing signals by synthesizing said first horizontal synchronizing signals which have been synchronized and internal horizontal synchronizing signals which have been generated inside said timing-generating circuit.

26. (New) A computer system according to claim 20, further comprising:

a decision circuit which decides a resolution of said image represented by said image signals, based on said first horizontal synchronizing signals and vertical synchronizing signals which have been inputted together with said image signals,

wherein said processing circuit enlarges said image represented by said image signals by a non-integer number of times in accordance with the resolution of said display panel divided by the resolution of said image represented by said image signals outputted from said computer main unit by using a decision result of said decision circuit.

27. (New) A computer system according to claim 26,  
further comprising:

a timing-generating circuit which generates display timing signals used on said display panel, based on said first horizontal synchronizing signals and said vertical synchronizing signals which have been inputted together with said image signals and the decision result of said decision circuit,

wherein said timing-generating circuit inputs said image signals whose image has been enlarged, and outputs said image signals together with said display timing signals on said display panel.

28. (New) A computer system according to claim 27,  
further comprising:

a bypass circuit which bypasses said memory and said processing circuit, and outputs said inputted image signals into said timing-generating circuit, when the resolution of said image represented by said image signals which have been inputted in accordance with the decision result of said decision circuit matches the resolution of said display panel.

29. (New) A computer system according to claim 20,

wherein said processing circuit is connected between said memory and said display panel, and

said processing circuit enlarges the image represented by said image signals which have been outputted from said memory by a non-integer number times.

30. (New) A computer system which enlarges an image represented by image signals to be displayed, comprising:

a computer main unit which outputs said image signals and horizontal synchronizing signals;

a memory which is arranged to store said image signals;

a display panel which displays said image represented by said image signals;

a processing circuit which enlarges the vertical direction of said image represented by said image signals by a non-integer number of times in accordance with a resolution of said image represented by said image signals outputted from said computer main unit; and

a control unit which outputs said image signals from said memory in accordance with an output timing synchronized with an input timing when said image signals are inputted into said memory,

wherein said control unit synchronizes said output timing with said input timing at designated intervals in accordance with a resolution of said display panel divided by a resolution of said image signals outputted from said computer unit, and

said output timing is generated at certain intervals.

31. (New) A computer system which enlarges an image represented by image signals to be displayed, comprising:

a computer main unit which outputs said image signals and first horizontal synchronizing signals;

a memory which is arranged to store said image signals;

a display panel which displays said image represented by said image signals;

a processing circuit which enlarges said image signal by a non-integer number of times in accordance with a resolution of said display panel divided by a resolution of said image represented by said image signals; and

a control circuit which inputs said image signals into said memory in accordance with said first horizontal synchronizing signals which have been inputted together with

said image signals, and outputs said image signals from said memory in accordance with second horizontal synchronizing signals synchronized with said first horizontal synchronizing signals,

wherein said control circuit synchronizes said second horizontal synchronizing signals with said first horizontal synchronizing signals, every time one of said first horizontal synchronizing signals is generated M times and one of said second horizontal synchronizing signals is generated N times,

N is not equal to M,

N divided by M is a non-integer number,

N divided by M corresponds to the resolution of said display panel divided by the resolution of said image represented by said image signals, and

each cycle of said second horizontal synchronizing signals is M divided by N times of each cycle of said first horizontal synchronizing signals.

32. (New) A display device which enlarges an image represented by image signals to be displayed, comprising:

a memory which is arranged to store said image signals;

a display panel which displays said image represented by said image signals;

a processing circuit which enlarges said image signal by a non-integer number of times in accordance with a resolution of said display panel divided by a resolution of said image represented by said image signals; and

a control circuit which inputs said image signals into said memory in accordance with first horizontal synchronizing signals which have been inputted together with said image signals, and outputs said image signals from said memory in accordance with second horizontal synchronizing signals synchronized with said first horizontal synchronizing signals,

wherein said control circuit synchronizes said second horizontal synchronizing signals with said first horizontal synchronizing signals, every time one of said first horizontal synchronizing signals is generated M times and one of said second horizontal synchronizing signals is generated N times,

N is not equal to M,

N divided by M is a non-integer number,

N divided by M corresponds to the resolution of said display panel divided by the resolution of said image represented by said image signals, and

a generation cycle of one of said second horizontal synchronizing signals is almost constant.

33. (New) A display device according to claim 32, wherein said memory is arranged to store said image signals for one frame.

34. (New) A display device according to claim 32, wherein said memory is arranged to store said image signals for two lines.

35. (New) A display device according to claim 32, wherein said processing circuit generates data which should be inserted into said image signals with a tone integral method.

36. (New) A display device according to claim 32, further comprising:

a timing-generating circuit which generates display timing signals used on said display panel, based on said first horizontal synchronizing signals and vertical synchronizing

signals which have been inputted together with said image signals, and

wherein said timing-generating circuit inputs said image signals whose image has been enlarged, and outputs said image signals on said display panel together with said display timing signals.

37. (New) A display device according to claim 36, wherein said timing-generating circuit comprises:

a synchronizing circuit which synchronizes said first horizontal synchronizing signals with a standard clock, and

a generating circuit which generates said second horizontal synchronizing signals by synthesizing said first horizontal synchronizing signals which have been synchronized and internal horizontal synchronizing signals which have been generated inside said timing generating circuit.

38. (New) A display device according to claim 32, further comprising:

a decision circuit which decides a resolution of said image represented by said image signals, based on said first horizontal synchronizing signals and vertical

synchronizing signals which have been inputted together with said image signals,

wherein said processing circuit enlarges said image represented by said image signals by a non-integer number of times in accordance with the resolution of said display panel divided by the resolution of said image represented by said image signals outputted by using a decision result of said decision circuit.

39. (New) A display device according to claim 38, further comprising:

a timing-generating circuit which generates display timing signals used on said display panel, based on said first horizontal synchronizing signals and said vertical synchronizing signals which have been inputted together with said image signals and the decision result of said decision circuit,

wherein said timing-generating circuit inputs said image signals whose image has been enlarged, and outputs said image signals together with said display timing signals on said display panel.

40. (New) A display device according to claim 39,  
further comprising:

a bypass circuit which bypasses said memory and said processing circuit, and outputs said inputted image signals into said timing-generating circuit, when the resolution of said image represented by said image signals which have been inputted in accordance with the decision result of said decision circuit matches the resolution of said display panel.

41. (New) A display device according to claim 32,

wherein said processing circuit is connected between said memory and said display panel, and

said processing circuit enlarges the image represented by said image signals which have been outputted from said memory by a non-integer number times.

42. (New) A display device which enlarges an image represented by image signals to be displayed, comprising:

a memory which is arranged to store said image signals;

a display panel which displays said image represented by said image signals;

a processing circuit which enlarges the vertical direction of said image represented by said image signals by a non-integer number of times in accordance with a resolution of said display panel divided by a resolution of said image represented by said image signals; and

a control unit which outputs said image signals from said memory in accordance with an output timing synchronized with an input timing when said image signals are inputted into said memory,

wherein said control unit synchronizes said output timing with said input timing at designated intervals in accordance with a resolution of said display panel divided by the resolution of said inputted image signals, and

said output timing is generated at certain intervals.

43. (New) A display device which enlarges an image represented by image signals to be displayed, comprising:

a memory which is arranged to store said image signals;

a display panel which displays said image represented by said image signals;

a processing circuit which enlarges said image signals by a non-integer number of times in accordance with a resolution of said display panel divided by a resolution of said image represented by said image signals; and

a control circuit which inputs said image signals into said memory in accordance with first horizontal synchronizing signals which have been inputted together with said image signals, and outputs said image signals from said memory in accordance with second horizontal synchronizing signals synchronized with said first horizontal synchronizing signals,

wherein said control circuit synchronizes said second horizontal synchronizing signals with said first horizontal synchronizing signals, every time one of said first horizontal synchronizing signals is generated M times and one of said second horizontal synchronizing signals is generated N times,

N is not equal to M,

N divided by M is a non-integer number,

N divided by M corresponds to the resolution of said display panel divided by the resolution of said image represented by said image signals, and

each cycle of said second horizontal synchronizing signals is  $M$  divided by  $N$  times of each cycle of said first horizontal synchronizing signals.